CLAIMS

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a first bus interface logic for coupling to a first external bus;

a microcontroller configured as an Alert Standard Format management engine, wherein the microcontroller is further configured to receive Alert Standard Format sensor data over the first external bus; and

a watchdog timer coupled to the microcontroller, wherein the watchdog timer is coupled to receive a reset input upon a predetermined change in a system state, wherein the watchdog timer is further configured to provide an indication to the microcontroller in response to an expiration of the watchdog timer.

2. The integrated circuit of claim 1, further comprising:

a second bus interface logic for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

3. The integrated circuit of claim 2, further comprising:

an embedded Ethernet controller coupled to the first internal bus.

4. The integrated circuit of claim 3, wherein the embedded Ethernet controller is configured to route the Alert Standard Format sensor data from the embedded Alert Standard Format management engine to an external management server.

5. The integrated circuit of claim 1, wherein the indication provided to the microcontroller includes a microcontroller interrupt.

6. The integrated circuit of claim 1, wherein the integrated circuit comprises a bridge, wherein the bridge further comprises:

a third bus interface logic for coupling to a second external bus.

7. The integrated circuit of claim 6, wherein the bridge comprises a south bridge, wherein the first external bus is configurable as a first input/output bus.

8. The integrated circuit of claim 7, wherein the first input/output bus is an SMBus.

9. The integrated circuit of claim 1, wherein the reset input is provided to the watchdog timer by the microcontroller.

10. The integrated circuit of claim 1, wherein the reset input is provided to the watchdog timer from an external processor.

11. The integrated circuit of claim 1, further comprising:

a register configured to store system status information.

12. The integrated circuit of claim 11, wherein the microcontroller is further configured to read the system status information from the register in response to the indication.

13. The integrated circuit of claim 12, wherein the microcontroller is further configured to provide the system status information to an external management server.

14. An integrated circuit, comprising:

means for coupling to a first external bus;

controller means configured as an Alert Standard Format management engine, wherein the controller means is further configured to receive Alert Standard Format sensor data over the first external bus; and

timing means coupled to the controller means, wherein the timing means is coupled to receive a reset input upon a predetermined change in a system state, wherein the timing means is further configured to provide an indication to the controller means in response to an expiration of the timing means.

15. The integrated circuit of claim 14, further comprising:

a second means for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

16. The integrated circuit of claim 15, further comprising:

an embedded networking means coupled to the first internal bus.

17. The integrated circuit of claim 16, wherein the embedded networking means is configured to route the Alert Standard Format sensor data from the embedded Alert Standard Format management engine to an external management means.

18. The integrated circuit of claim 14, wherein the indication provided to the controller means includes an interrupt.

19. The integrated circuit of claim 14, wherein the integrated circuit comprises a bridge, wherein the bridge further comprises:

a third means for coupling to a second external bus.

20. The integrated circuit of claim 19, wherein the bridge comprises a south bridge, wherein the first external bus is configurable as a first input/output bus.

21. The integrated circuit of claim 20, wherein the first input/output bus is an SMBus.

22. The integrated circuit of claim 14, wherein the reset input is provided to the timing means by the controller means.

23. The integrated circuit of claim 14, wherein the reset input is provided to the timing means from an external processing means.

24. The integrated circuit of claim 14, further comprising:

a storage means configure to store system status information.

25. The integrated circuit of claim 24, wherein the controller means is further configured to read the system status information from the storage means in response to the indication.

26. The integrated circuit of claim 25, wherein the controller means is further configured to provide the system status information to an external management means.

16. A client computer system, comprising:

a first external bus;

an integrated circuit, comprising:

a first bus interface logic for coupling to the first external bus;

a microcontroller configured as an Alert Standard Format management engine, wherein the microcontroller is further configured to receive Alert Standard Format sensor data over the first external bus; and

a watchdog timer coupled to the microcontroller, wherein the watchdog timer is coupled to receive a reset input upon a predetermined change in a system state, wherein the watchdog timer is further configured to provide an indication to the microcontroller in response to an expiration of the watchdog timer.

17. The client computer system of claim 16, the integrated circuit further comprising:

a first internal bus; and

a second bus interface logic for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

18. The client computer system of claim 17, the integrated circuit further comprising:

an embedded Ethernet controller coupled to the first internal bus.

19. The client computer system of claim 18, wherein the embedded Ethernet controller is configured to route the Alert Standard Format sensor data from the embedded Alert Standard Format management engine to an external management server.

20. The client computer system of claim 16, wherein the indication provided to the microcontroller comprises a microcontroller interrupt.

21. The client computer system of claim 16, wherein the integrated circuit comprises a bridge, wherein the bridge further comprises:

a third bus interface logic for coupling to a second external bus.

22. The client computer system of claim 21, wherein the bridge comprises a south bridge, wherein first external bus is configurable as a first input/output bus.

23. The client computer system of claim 22, wherein the first input/output bus is an SMBus.

24. The client computer system of claim 16, wherein the reset input is provided to the watchdog timer by the microcontroller.

25. The client computer system of claim 16, further comprising:

a processor configured to provide the reset input to the watchdog timer.

26. The client computer system of claim 16, wherein the integrated circuit further comprises:

a register configured to store system status information.

27. The client computer system of claim 26, wherein the microcontroller is further configured to read the system status information from the register in response to the indication.

28. The client computer system of claim 27, wherein the microcontroller is further configured to provide the system status information to an external management server.

22. A method for operating an integrated circuit in a computer system, the method comprising:

entering a system state in the computer system;

resetting a watchdog timer on the integrated circuit;

determining an expiration of the watchdog timer on the integrated circuit;

evaluating the system state in the computer system; and

determining a system error in the computer system; and

responding to the system error by a microcontroller on the integrated circuit.

23. The method of claim 22, wherein resetting the watchdog timer on the integrated circuit comprises resetting the watchdog timer on the integrated circuit in response to entering the system state in the computer system.

24. The method of claim 22, wherein evaluating the system state in the computer system comprises evaluating the system state in the computer system in response to determining the expiration of the watchdog timer on the integrated circuit.

25. The method of claim 22, further comprising:

storing an indication of the system state.

26. The method of claim 25, wherein storing the indication of the system state comprises storing the indication of the system state in a storage location on the integrated circuit.

27. The method of claim 25, wherein storing the indication of the system state comprises storing the indication of the system state in response to entering the system state in the computer system.

28. The method of claim 25, wherein evaluating the system state in the computer system comprises reading the indication of the system state.

29. A computer readable medium encoded with instructions that, when executed by a client computer system, performs a method for operating an integrated circuit in the client computer system, the method comprising:

entering a system state in the computer system;

resetting a watchdog timer on the integrated circuit;

determining an expiration of the watchdog timer on the integrated circuit;

evaluating the system state in the computer system; and

determining a system error in the computer system; and

responding to the system error by a microcontroller on the integrated circuit.

30. The computer readable medium as set forth in claim 29, wherein resetting the watchdog timer on the integrated circuit comprises resetting the watchdog timer on the integrated circuit in response to entering the system state in the computer system.

31. The computer readable medium as set forth in claim 29, wherein evaluating the system state in the computer system comprises evaluating the system state in the computer system in response to determining the expiration of the watchdog timer on the integrated circuit.

32. The computer readable medium as set forth in claim 29, the method further comprising: storing an indication of the system state.

33. The computer readable medium as set forth in claim 32, wherein storing the indication of the system state comprises storing the indication of the system state in a storage location on the integrated circuit.

34. The computer readable medium as set forth in claim 32, wherein storing the indication of the system state comprises storing the indication of the system state in response to entering the system state in the computer system.

35. The computer readable medium as set forth in claim 32, wherein evaluating the system state in the computer system comprises reading the indication of the system state.

36. A method for operating an integrated circuit in a computer system, the method comprising the steps of:

entering a system state in the computer system;

resetting a watchdog timer on the integrated circuit;

determining an expiration of the watchdog timer on the integrated circuit;

evaluating the system state in the computer system; and

determining a system error in the computer system; and

responding to the system error by a microcontroller on the integrated circuit.

37. The method of claim 36, wherein resetting the watchdog timer on the integrated circuit comprises resetting the watchdog timer on the integrated circuit in response to entering the system state in the computer system.

38. The method of claim 36, wherein evaluating the system state in the computer system comprises evaluating the system state in the computer system in response to determining the expiration of the watchdog timer on the integrated circuit.

39. The method of claim 36, further comprising the step of:

storing an indication of the system state.

40. The method of claim 39, wherein storing the indication of the system state comprises storing the indication of the system state in a storage location on the integrated circuit.

41. The method of claim 39, wherein storing the indication of the system state comprises storing the indication of the system state in response to entering the system state in the computer system.

42. The method of claim 39, wherein evaluating the system state in the computer system comprises reading the indication of the system state.